**REMARKS** 

In the Office Action, the Examiner rejected claim 1 for containing ambiguous terms. The

Examiner rejected claims 1-15 under § 102 as being anticipated by USP 6,407,434 issued to

Rostoker et al. (Rostoker). In this Amendment, Applicants have amended claims 1, 2, 4, 5, 8, and

12. No claims have been deleted or added. Accordingly, claims 1-15 will be pending after entry of

this Amendment.

I. Informalities

In this Amendment, Applicants have amended claims 5 and 12 to correct certain

informalities in these claims.

II. Ambiguous Terms

The Examiner rejected claim 1 because the terms "set of potential sub-regions" were

ambiguous. Applicants have removed the term "potential" from the claim. In view of the

foregoing, Applicants respectfully request reconsideration and withdrawal of the objection to the

claims for the use of the term "potential."

III. Claims 1-7

The Examiner rejected claims 1-7 under § 102 as being anticipated by Rostoker.

Claims 2-7 are dependent directly or indirectly on independent claim 1. Claim 1 recites a

method of pre-computing costs of placing circuit modules in regions of circuit layouts. This

method defines a set of partitioning lines for partitioning the region into a plurality of sub-regions

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during a placement operation. For each set of sub-regions, the method then identifies a connection

graph that traverses the set of sub-regions, where some of the connection graphs have edges that

are at least partially diagonal. The method identifies an attribute of each identified connection

graph. For each set of sub-regions, the method then stores the attribute of the connection graph

identified for the set. The stored attribute is for use during a placement operation to compute

costs of placing circuit modules in regions of circuit layouts.

Applicants respectfully submit that Rostoker does not disclose teach, or even suggest

such a method. Specifically, Applicants respectfully submit that Rostoker does not disclose a

method that:

• for a set of sub-regions, identifies a connection graph that connects the set of sub-

regions, wherein the connection graph has at least one edge that is at least partially

diagonal;

• for each set of sub-regions, identifies a connection graph that traverses the set of

sub-regions, wherein some of the connection graphs have edges that are at least

partially diagonal;

• identifies an attribute of each identified connection graph; and

for each set of sub-regions, stores the attribute of the connection graph identified

for the set, where the attribute is for use during a placement operation to compute

costs of placing circuit modules in regions of circuit layouts.

The Examiner identifies column 59, lines 44-60 of Rostoker as disclosing the storing

element of claim 1. However, as characterized by the Examiner, this passage of Rostoker

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discloses a "routing graph connection storage" implemented during a routing operation. This

routing operation as disclosed in Rostoker transpires after a placement operation. Therefore,

Rostoker does not disclose, teach or even suggest the recited method of claim 1, which pre-

computes costs of placing circuit modules in regions of circuit layouts. To add further force and

reasoning to this argument, Applicants have amended claim 1 to recite that the stored attribute is

for use during a placement operation to compute costs of placing circuit modules in regions of

circuit layouts.

Accordingly, Applicants respectfully submit that Rostoker does not render claim 1

unpatentable. As claims 2-7 are dependent on claim 1, Applicants respectfully submit that claims

2-7 are patentable over Rostoker for at least the same reasons. In view of the foregoing,

Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims

1-7.

IV. Claims 8-15

The Examiner rejected claims 8-15 under § 102 as being anticipated by Rostoker.

Claims 9-15 are dependent directly or indirectly on independent claim 8. Claim 8 recites a

method of computing placement costs for a placer that partitions a region of a circuit layout into

a plurality of sub-regions. This method identifies, for a set of sub-regions, a connection graph

that connects the set of sub-regions, where the connection graph has at least one edge that is at

least partially diagonal. The method identifies a placement cost from an attribute of the

connection graph. The method then stores the placement cost for the set of sub-regions. The

placement cost is for use during a placement operation to compute costs of placing circuit

Attny Docket: SPLX.P0126 PTO Serial Number: 10/079,061 modules in regions of circuit layouts.

Applicants respectfully submit that Rostoker does not disclose teach, or even suggest

such a method. Specifically, Applicants respectfully submit that Rostoker does not disclose a

method that:

defines a set of partitioning lines for partitioning the region into a plurality of sub-

regions during a placement operation;

• identifies a placement cost from an attribute of the connection graph;

identifies an attribute of each identified connection graph; and

stores the placement cost for the set of sub-regions, where the placement cost is

for use during a placement operation to compute costs of placing circuit modules

in regions of circuit layouts.

The Examiner identifies column 59, lines 44-60 of Rostoker as disclosing the storing

element of claim 8. However, as characterized by the Examiner, this passage of Rostoker

discloses a "routing graph connection storage" implemented during a routing operation. This

routing operation as disclosed in Rostoker transpires after a placement operation. Therefore,

Rostoker does not disclose, teach or even suggest the recited method of claim 8, which computes

placement costs for a placer that partitions a region of a circuit layout into a plurality of sub-

regions. To add further force and reasoning to this argument, Applicants have amended claim 8 to

recite that the stored placement cost is for use during a placement operation to compute costs of

placing circuit modules in regions of circuit layouts.

Attny Docket: SPLX.P0126 PTO Serial Number: 10/079,061 Accordingly, Applicants respectfully submit that Rostoker does not render claim 8 unpatentable. As claims 9-15 are dependent on claim 8, Applicants respectfully submit that claims 9-15 are patentable over Rostoker for at least the same reasons. In view of the foregoing, Applicants respectfully request reconsideration and withdrawal of the § 102 rejection of claims 8-15.

## CONCLUSION

In view of the foregoing, it is submitted that all pending claims, namely claims 1-15, are in condition for allowance. Reconsideration of the rejections and objections is requested. Allowance is earnestly solicited at the earliest possible date.

Respectfully submitted,

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Dated: 6 (1/8

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